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RISC-V Server Feature in SpacemiT SoCs

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RISC-V Server IP Racks

- Server SoC Platform – V100
  - 64-core X100
  - Support CPU/IO virtualization
  - Support BMC/UEFI server firmware environment
  - Support RISC-V compliant RAS and perf features
  - Support trusted computing
- High Performance CPU – X100
  - SPEC CPU@ 2006 scores > 9/GHz
  - 2.5GHz@12nm
  - AI computers and AI robots
- High Performance CPU – X200
  - SPEC CPU@ 2006 scores > 16/GHz
  - 3.2GHz@7nm
  - Super AI computers, cloud computing and advanced automotive chips

RISC-V Server SoC Compliance

Segment	Required	Supported
timers		All compliant
AIA		All compliant
IOMMU	SHOULD support MRIF	No MRIF support
	SHOULD support DBG	No DBG support
PCIe	MUST support ACS I/O request blocking	No ACS enhanced capability
	SHOULD support P2P VDM routing between RCs	No P2P VDM routing between RCs except MCTP routing
	MAY support P2P VDM routing between EPs	No P2P VDM routing between EPs
	MAY support PTM	No PTM support
RAS		All compliant
QoS	SHOULD support CBQRI	No CBQRI support

- **Compliant to RISC-V Server SoC Specification v1.0, 2025-02-21: Ratified**
- **Support all but one PCIe 6.0 MUST feature**
- **Support most SHOULD features and lots of MAY features**
- **Significant compliance to virtualization, manageability (RAS), security, performance requirements**

Segment	Required	Supported
Manageability		All compliant
Performance Monitoring	SHOULD support requester average latency counting	Only support target latency counting
	SHOULD support local/remote filter	No local/remote filter
	SHOULD support PCIe flit performance measurement	No PCIe flit performance measurement
Security	SHOULD support PCIe IDE	No PCIe IDE
	SHOULD support off-chip DRAM encryption	No off-chip DRAM encryption

Contents

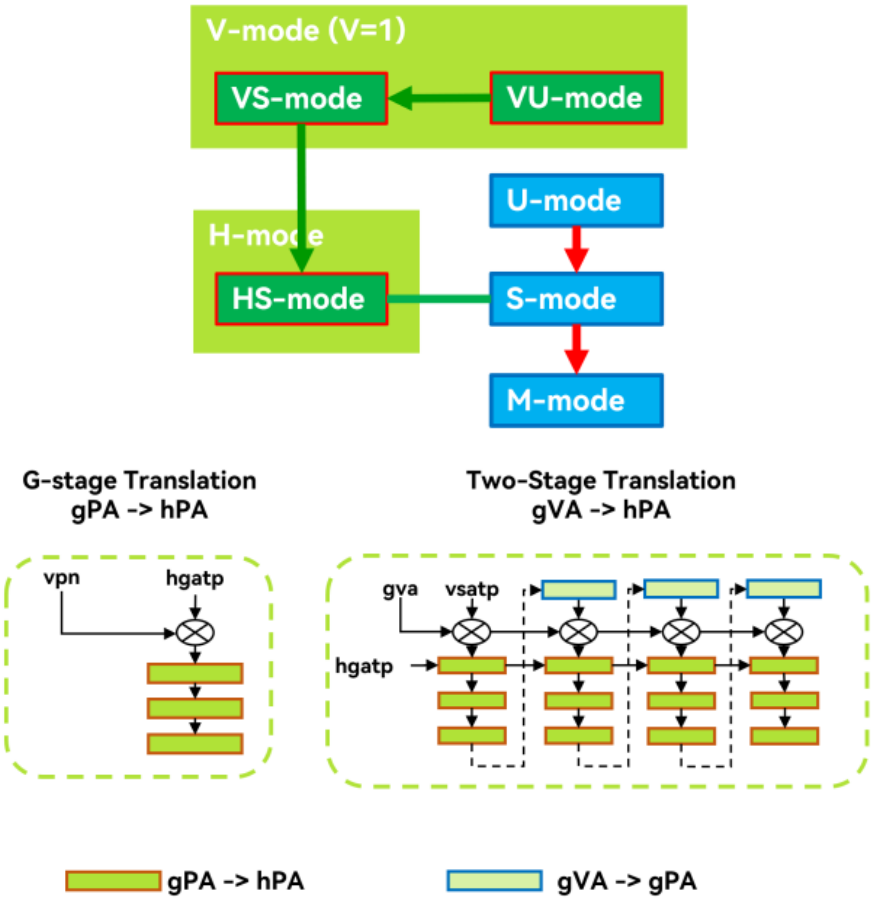
01 Virtualization
02 Manageability
03 Security
04 Performance
05 Other features

01

Virtualization

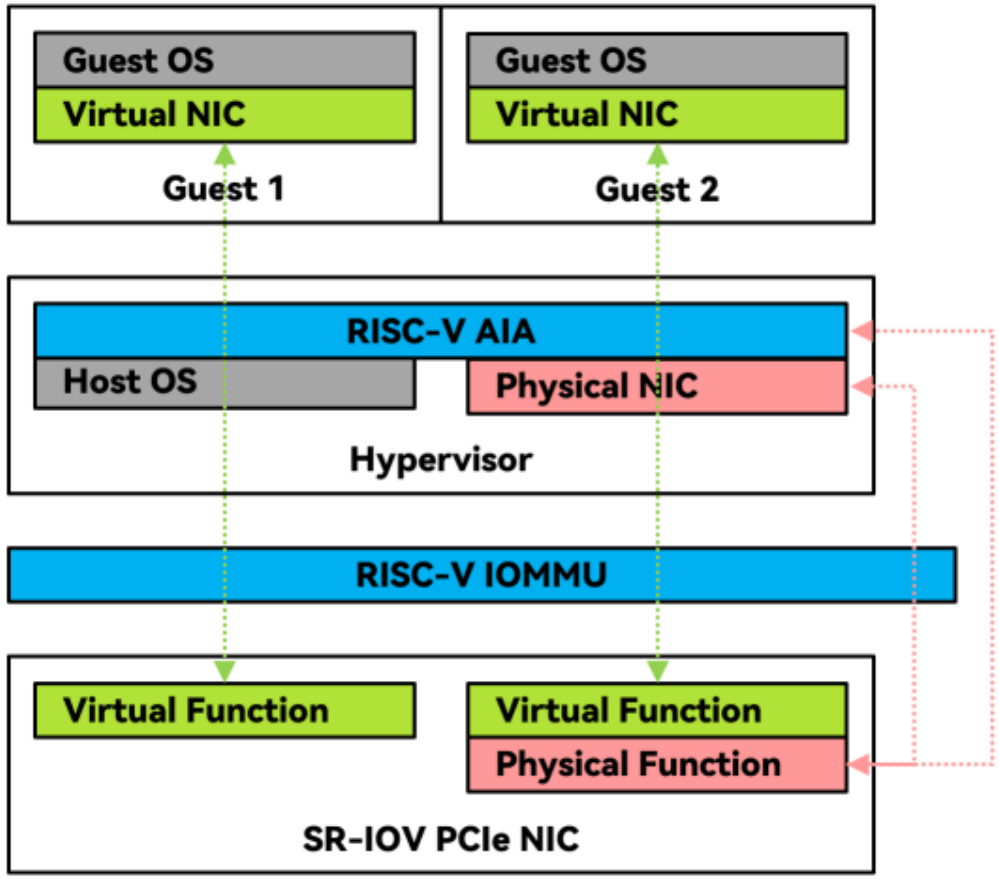
CPU Virtualization – RVH

- Hypervisor extended S (HS) mode
  - HS-mode CSR, time delta HPM
  - Guest page/virtual instruction fault/HS-mode ECALL
  - VSEI/VSTI/VSSI
- Virtualization Mode (V)
  - Virtualized supervisor (VS) mode/Virtualized user (VU) mode
  - VS-mode background CSR
  - ECALL from VS-mode/VU-mode
- Address translations
  - hgatp pointing to G-stage translation table
  - vsatp pointing to VS-stage translation table
  - PTW/TLB with GPA support
- Instructions
  - HS-mode system barrier
  - Guest memory access

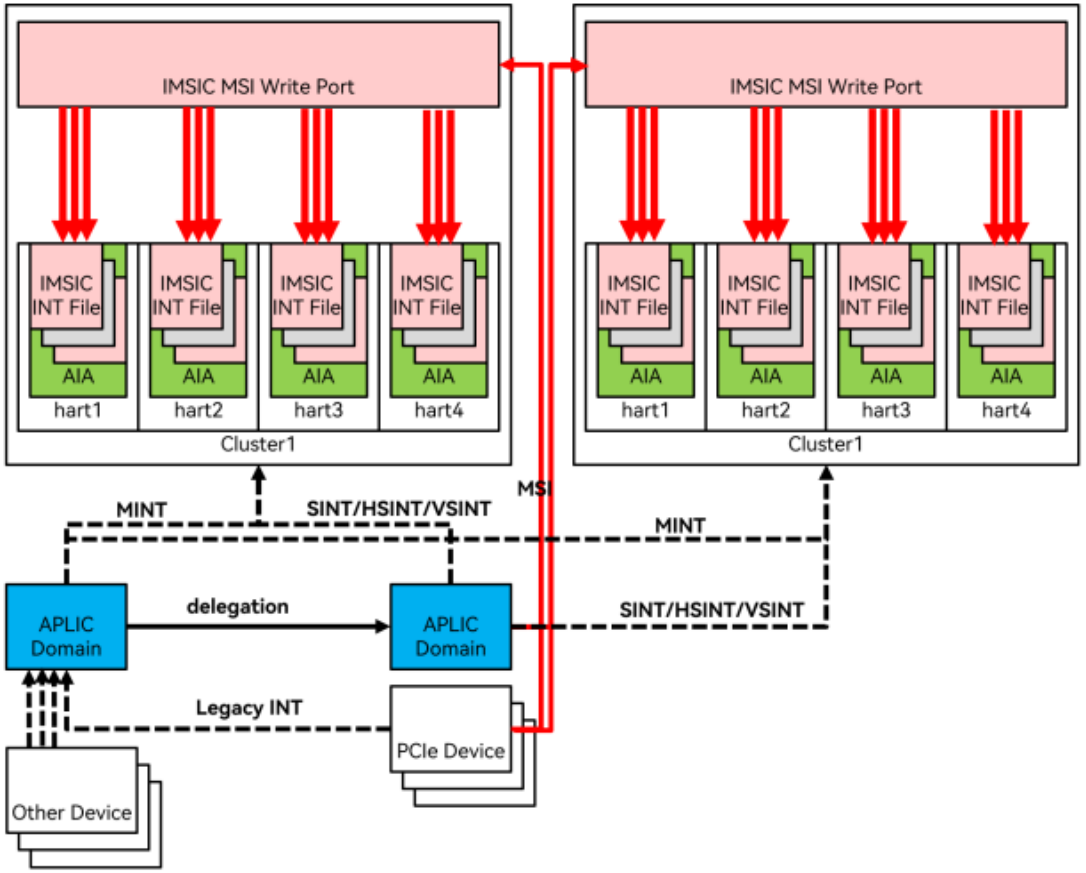


IO Virtualization Overview

- IO virtualization – AIA
- IO virtualization – IOMMU
- IO virtualization – SR-IOV
  - Support PCIe physical function assignment of host OS
  - Support PCIe virtual function assignment of guest OS

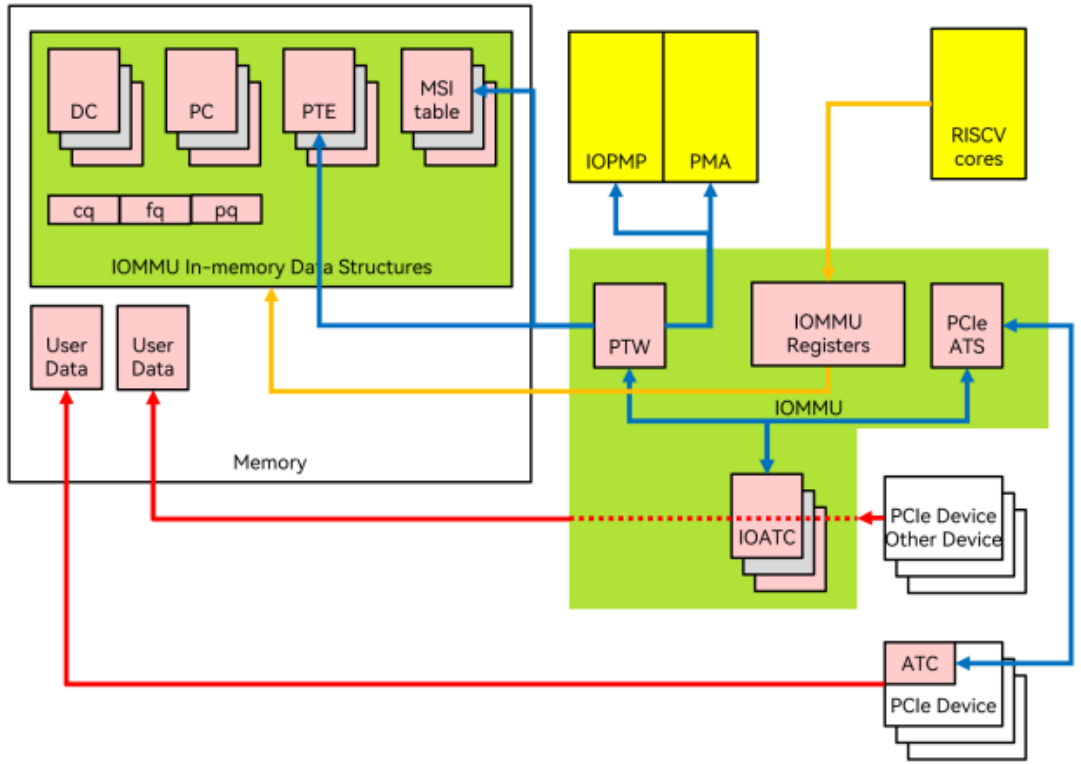


IO Virtualization – AIA



- AIA v1.0 compliant
  - Major IRQ priority
  - Virtual interrupt, VTI
  - GEILEN >= 8
  - WSI and MSI support
  - 1023 APLIC interrupt sources
  - 2048 IMSIC interrupt sources
- Prioritized platform IRQs:
  - RAS CE, RAS NE, NMI, debug and trace, etc.
- MSI support
- PCIe interrupt routing
- IRQ virtualization and remapping
- Interrupt domain
- GSI/IPI support

IO Virtualization – IOMMU



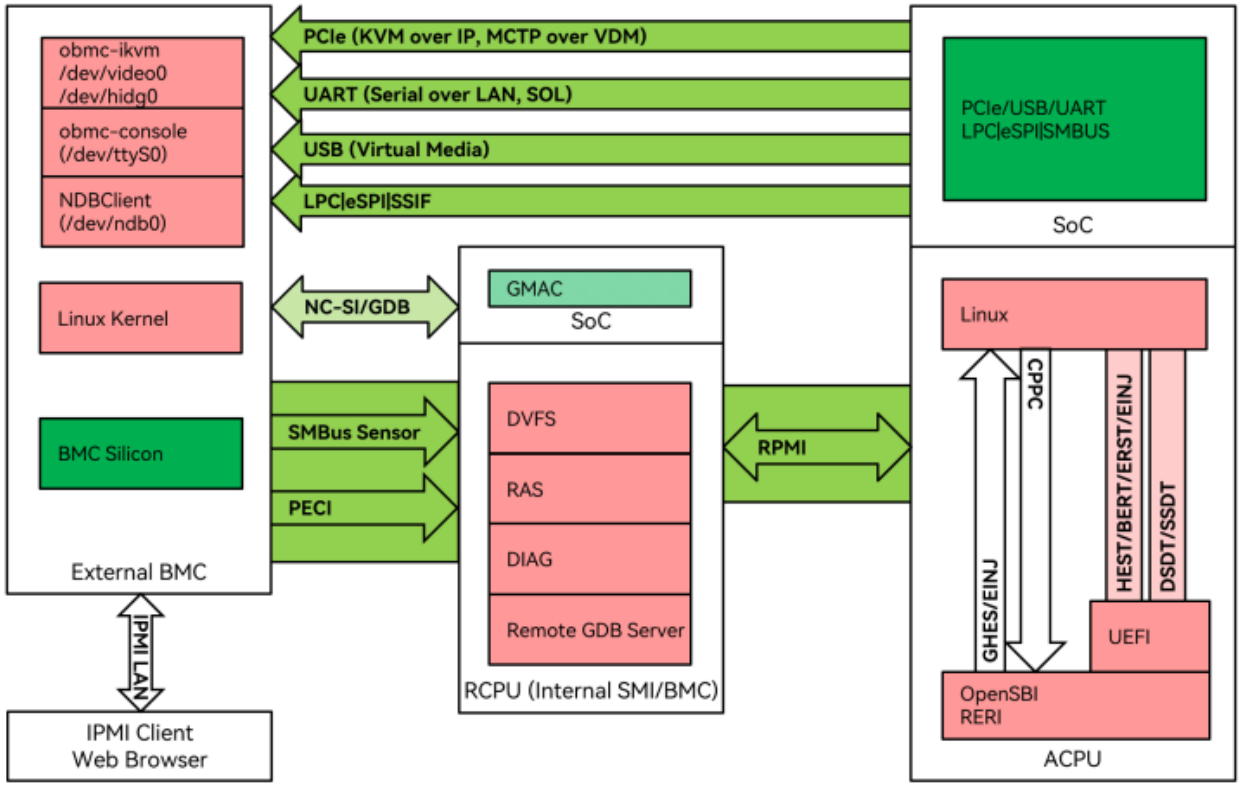
- IOMMU v1.0 Compliant **T100**
  - **24-bit DDI**, **20-bit PDI**, 44-bit DMA
  - Sv39/Sv48 S1 + Sv39x4 Sv48x4 S2 support
  - PCIe ATS/T2GPA/PRI support
  - Support MSI flat, Svpbmt/Svnapot
  - **Support HPM and RAS RERI**
  - Support IOPMP/PMA check
- Interrupt remapping and virtualization
- DMA remapping, memory protection
- Pointer-is-a-Pointer in heterogenous computing (accelerators)
- Nested address translation in Guest OS
- Translation Cache in PCIe device
- Demand Paging from PCIe device

02

Manageability

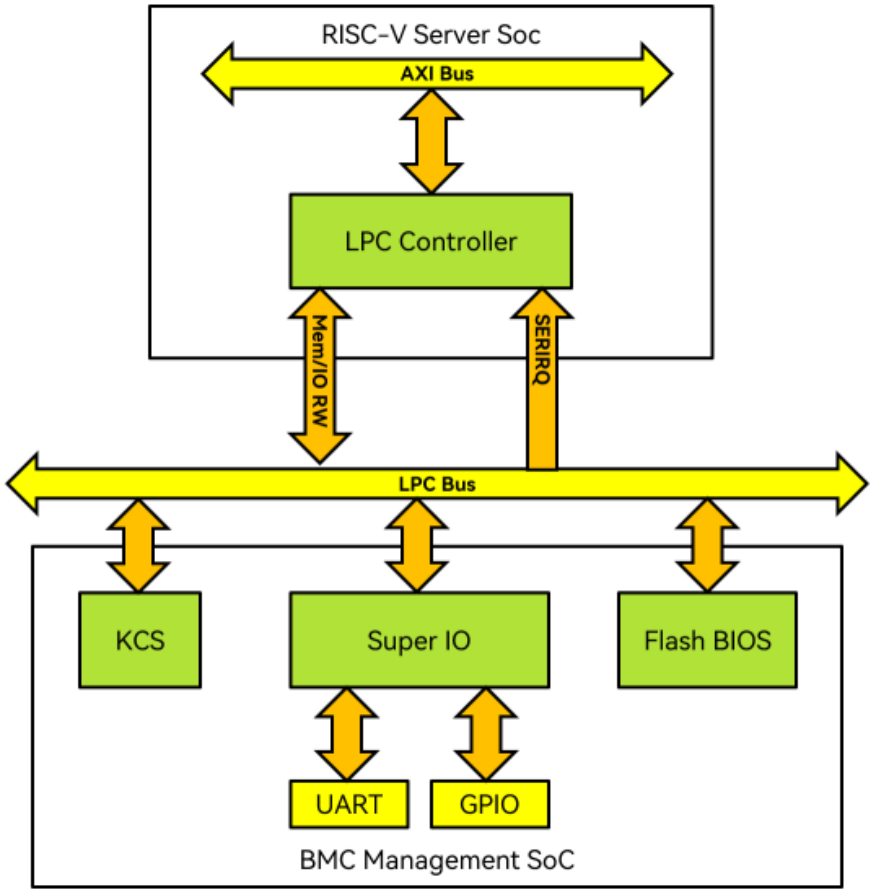
Manageability Overview

- BMC features
  - LPC
  - eSPI
  - KCS
  - SSIF
  - SOL
  - KVM
  - MCTP
  - PECI
- DVFS ACPI compliance
  - CPPC
- DVFS RISC-V compliance
  - RPMI



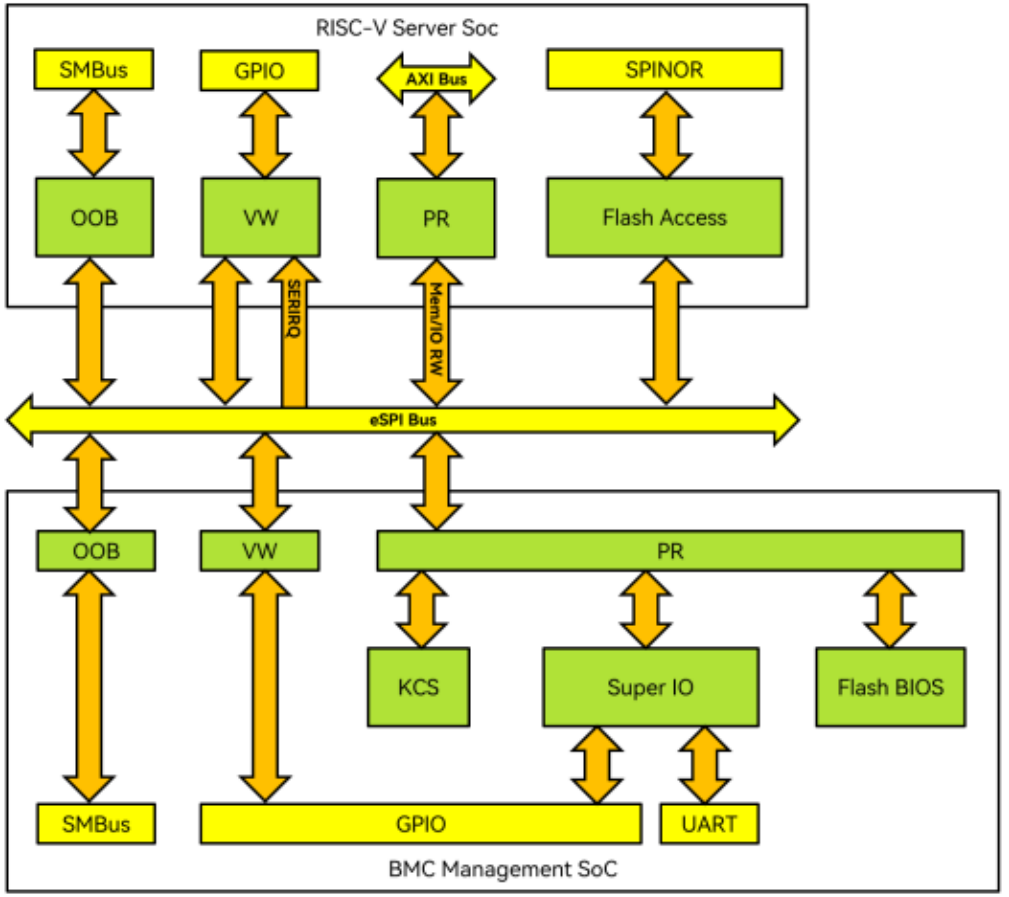
BMC Feature – LPC

- Intel Low PIN Count Interface 1.1
- Support I/O, memory and firmware read/write cycle
- Support 1/2/4 bytes firmware read/write cycle
- Support 17 ~ 32 IRQ slots SERIRQ interface
- Support AXI4 64-bit address, 32-bit data width, 64KB bridged I/O space and 32MB bridged memory space



BMC Feature – eSPI

- Enhanced Serial Peripheral Interface (eSPI) revision 1.0
- Support PR/OOB/VW/flash access channels
- Support 20/25/33/50/66MHz IO frequency
- Support 1x/2x/4x eSPI I/O mode
- Support AXI4 64-bit address, 32-bit data width, burst 16, 64KB bridged I/O space and 32MB bridged memory space
- Support 16*4-byte PR FIFO size
- Support 0-23 VW IRQ, up to 16-bit GPIO
- Support interrupt for system event 2~7
- Support up to 16 VW count per transfer
- Support up to 128-byte OOB and flash access transfer size



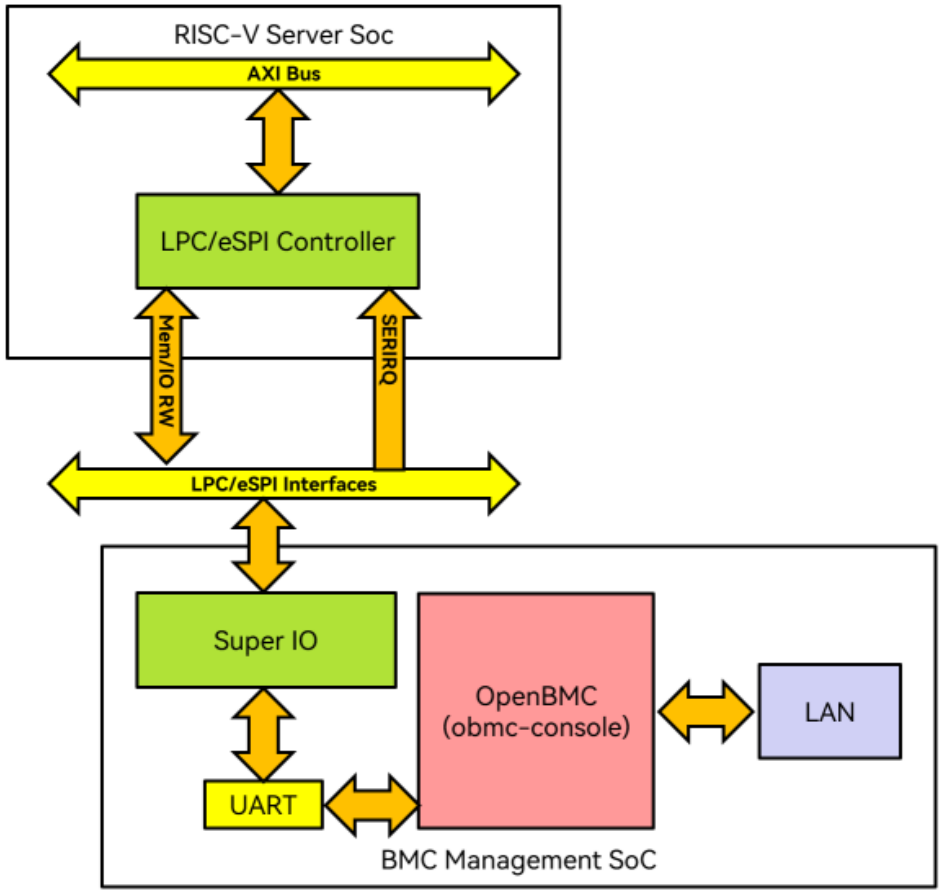
BMC Feature – KCS/SSIF

- Support traditional non-x86 platform IPI0001 PnP device returning _IFT 0x04 SSIF via SMBus
- Support IPI0001 PnP device returning _IFT 0x01 KCS IPMI system interface KCS via LPC I/O and eSPI PR channel
- Support ACPI IPMI operation region in system definition tables
- Support accesses to BMC power meters

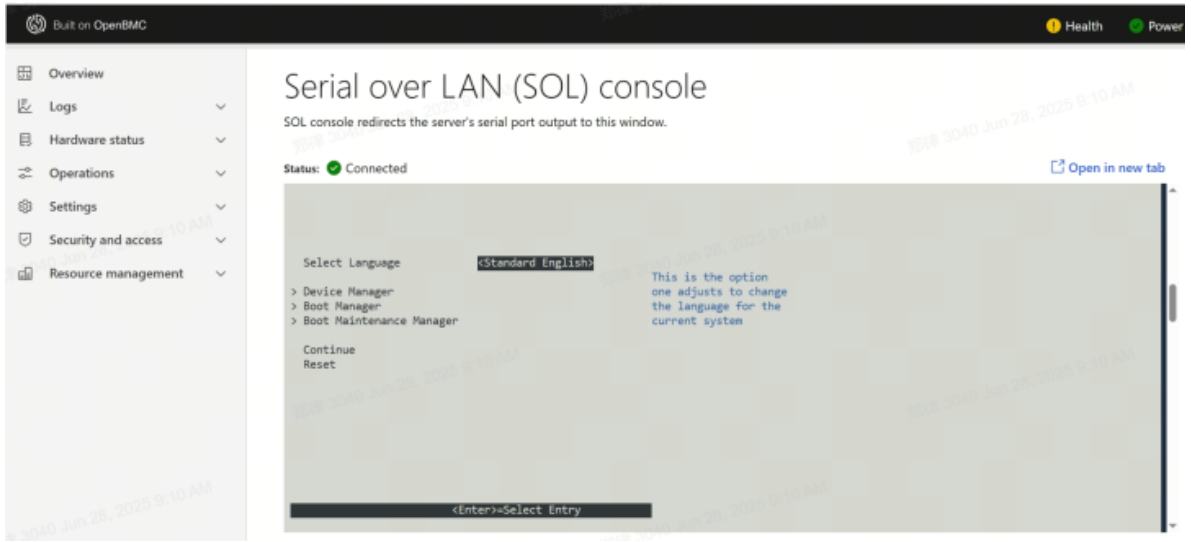
```
[    5.429923] riscv-aplic RSCV0002:00: 511 interrupts forwarded to MSI base 0x0
000000558600000
[    5.468665] IPMI message handler: version 39.2
[    5.481225] ipmi device interface
[    5.670716] ipmi_si: IPMI System Interface driver
[    5.688403] ipmi_si IPI0001:00: ipmi_platform: probing via ACPI
[    5.706054] ipmi_si IPI0001:00: ipmi_platform: [mem 0x53fe00ca2 window] regsi
ze 1 spacing 1 irq 13
[   82.322779] Freeing initrd memory: 18476K
[   82.424998] ipmi_si: Adding ACPI-specified kcs state machine
[   82.444542] ipmi_si: Trying ACPI-specified kcs state machine at mem address 0
x53fe00ca2, slave address 0x0, irq 13
[   83.084217] ipmi_si IPI0001:00: The BMC does not support clearing the recv ir
q bit, compensating, but the BMC needs to be fixed.
[   83.628675] ipmi_si IPI0001:00: Using irq 13
[   83.759773] ipmi_si IPI0001:00: Error clearing flags: c1
[   84.498262] ipmi_si IPI0001:00: IPMI message handler: Found new BMC (man_id:
0x00a741, prod_id: 0x424f, dev_id: 0x00)
[   87.328451] ipmi_si IPI0001:00: IPMI kcs interface initialized
[   89.942581] Serial: 8250/16550 driver, 4 ports, IRQ sharing disabled
[   90.031293] serial8250 RSCV0003:00: error -ENXIO: IRQ index 0 not found
```

```
sdfirm> kcs xfer 2 63 0x6 0x1
00000000  0000000000000106 0000000000000000  |................|
00000010  0000000000000000 0000000000000000  |................|
Command success 'kcs - 0'
```

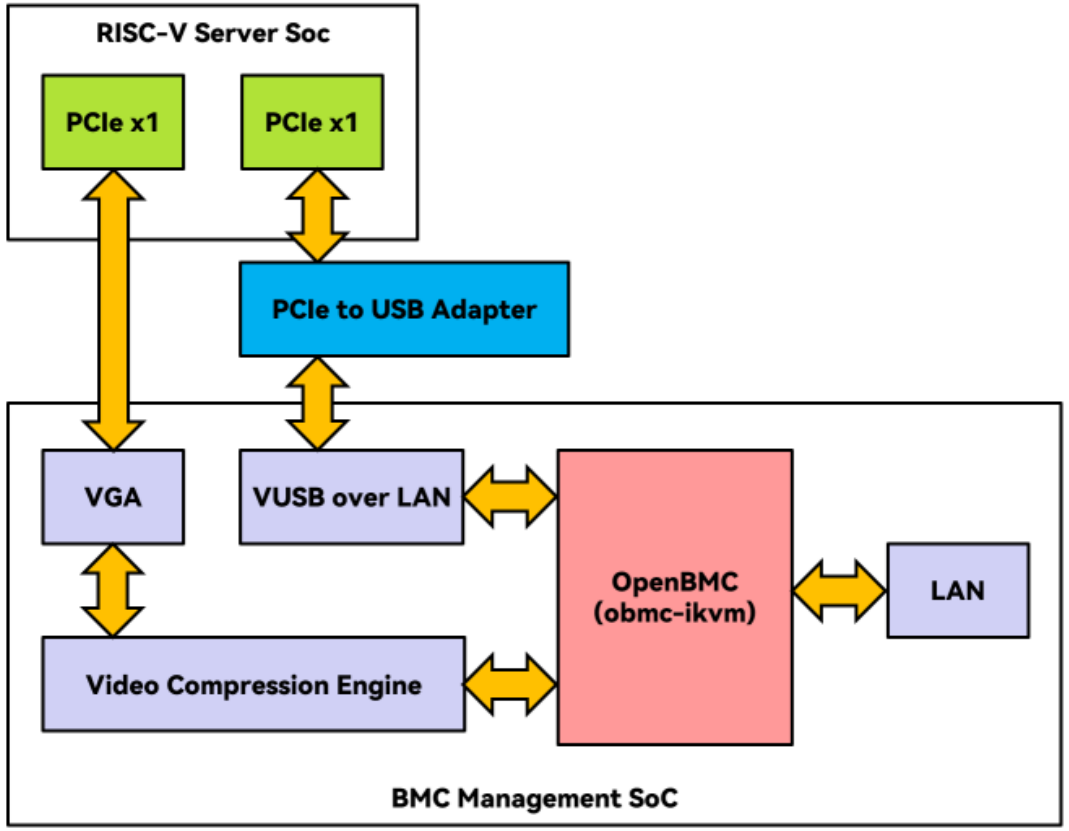
BMC Feature – SOL



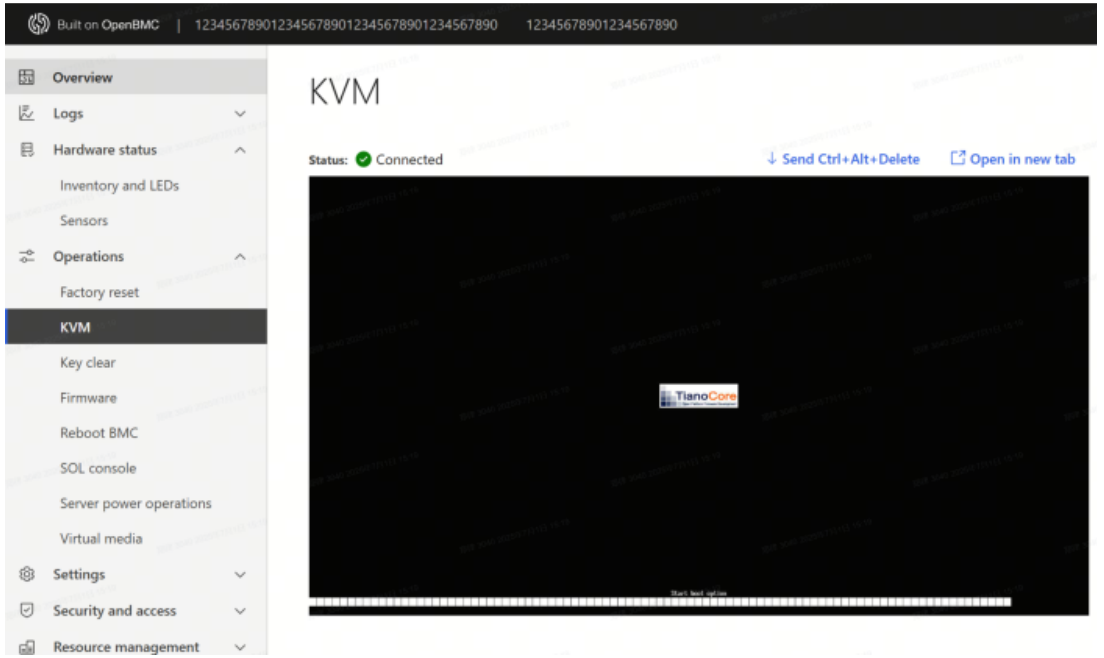
- Support remote OS install, BIOS setup, etc. using CUI
- Enable BMC IPMI SOL (serial over LAN) console using LPC/eSPI adapters
- Support super IO peripherals in UEFI
- Support UART based on SIO/SERIRQ in UEFI



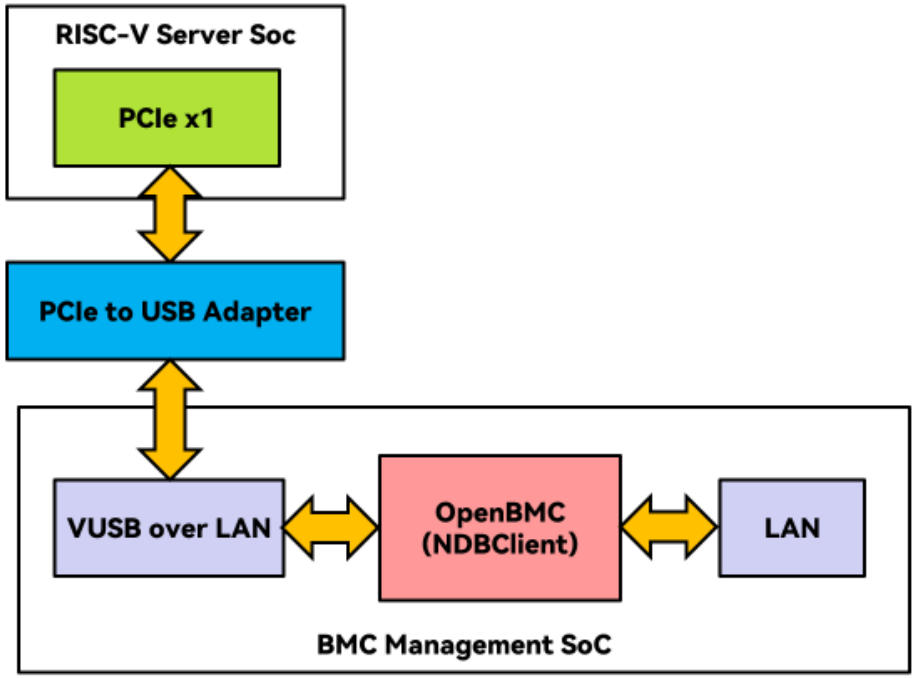
BMC Feature – KVM



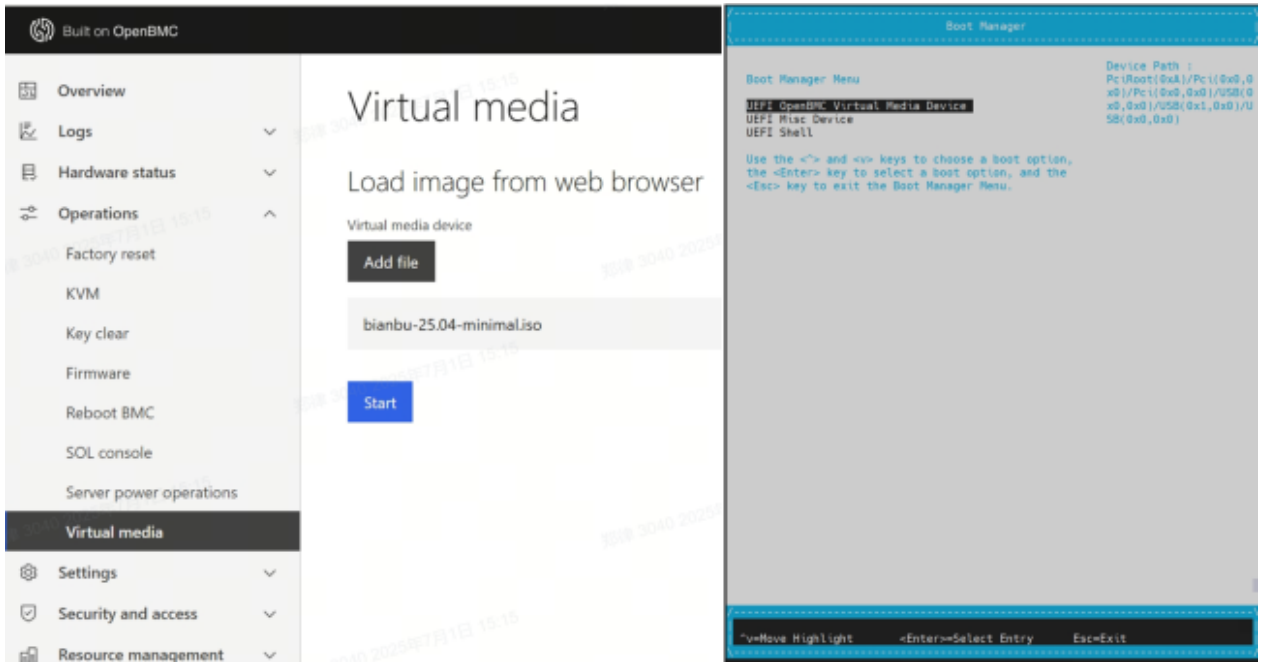
- Support remote OS install, BIOS setup, etc. using GUI
- Enable BMC KVM (keyboard, video, mouse) over IP using dedicated PCIe adapters
- Support USB over LAN protocol using virtual USB
- Support graphics compression into YUV420/YUV444



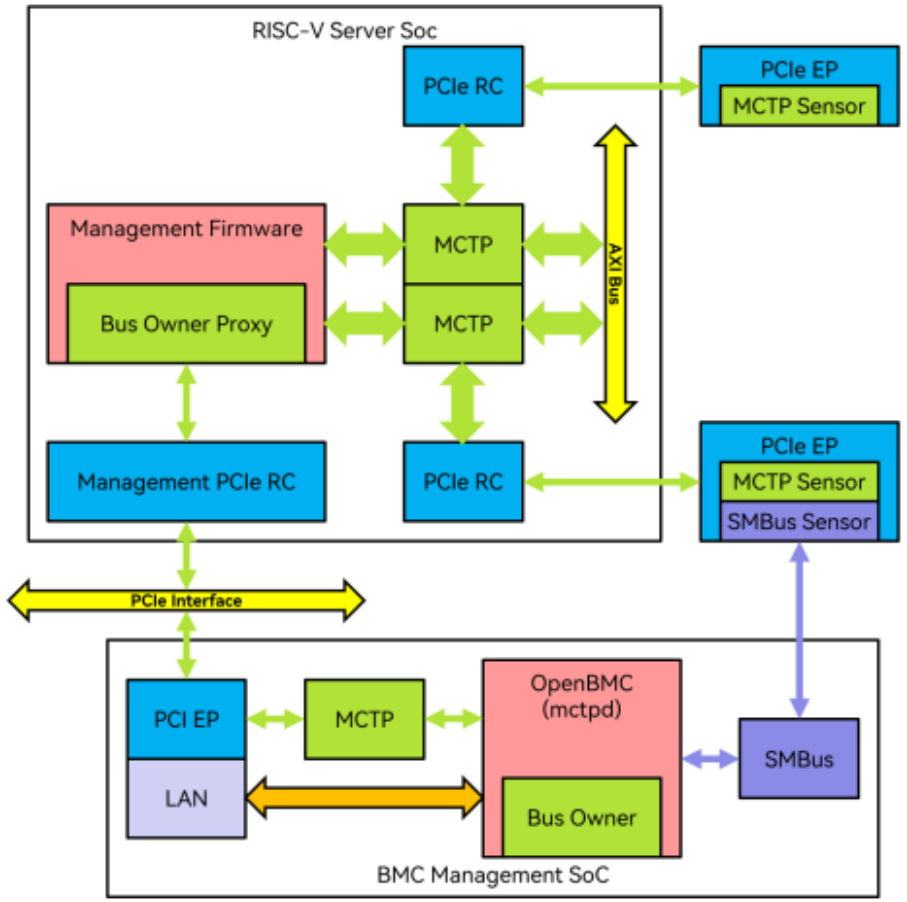
BMC Feature – Virtual Media



- Support remote operating system installation along with SOL and KVM
- Enable BMC USB virtual media using dedicated PCIe adapters
- Support USB over LAN protocol using virtual USB



BMC Feature – MCTP

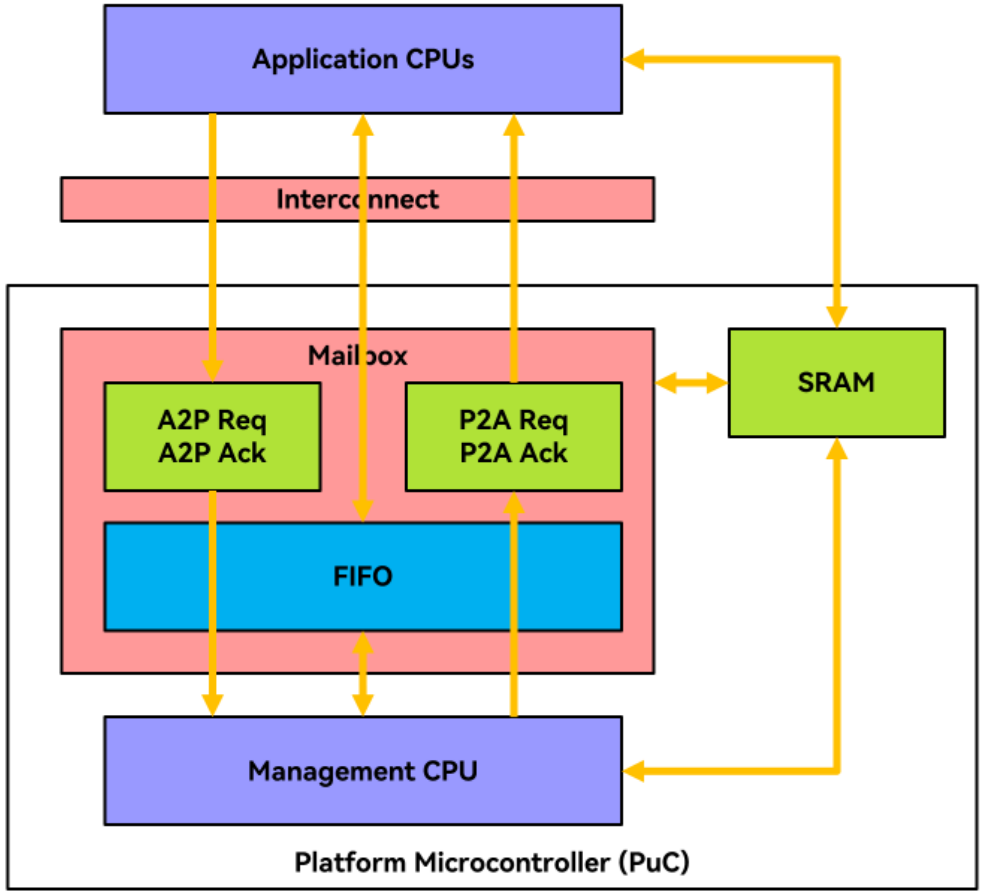



```
mctp[10] recv size: 20
get data:
410132808  01 10 00 73 7f 10 00 01  b4 1a 00 00 c8 08 ff 01  |...s............|
410132818  00 80 0b 00                                       |....|

recv mctp command[11]: Prepare Endpoint Discovery ctrl->rq: 1
tx status: 0x9
mctp[0] send done, size: 20
j_mctp[0] send size: 20



mctp[0] recv size: 20
get data:
410132808  01 00 00 70 7f 00 00 01  b4 1a 00 00 c0 00 08 01  |...p............|
410132818  00 00 0b 00                                       |....|

recv mctp command[11]: Prepare Endpoint Discovery ctrl->rq: 0
tx status: 0x9
mctp[10] send done, size: 20
j_mctp[10] send size: 20
----------
mctppcie0 Link encap:UNSPEC  HWaddr 00-00-30-30-30-30-00-30-00-00-00-00-00-00-00-00
          UP RUNNING  MTU:1024  Metric:1
          RX packets:3 errors:0 dropped:0 overruns:0 frame:0
          TX packets:3 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1100
          RX bytes:432 (432.0 B)  TX bytes:64 (64.0 B)
```

- Management firmware programs PCIe VDM routing to/from AXI memory between RCs
- Management firmware acts as MCTP bus owner proxy and BMC acts as MCTP bus owner and bridge
- Demonstration:
  - MCTP EP discovery request and response
  - MCTP probed interface on BMC evaluation board

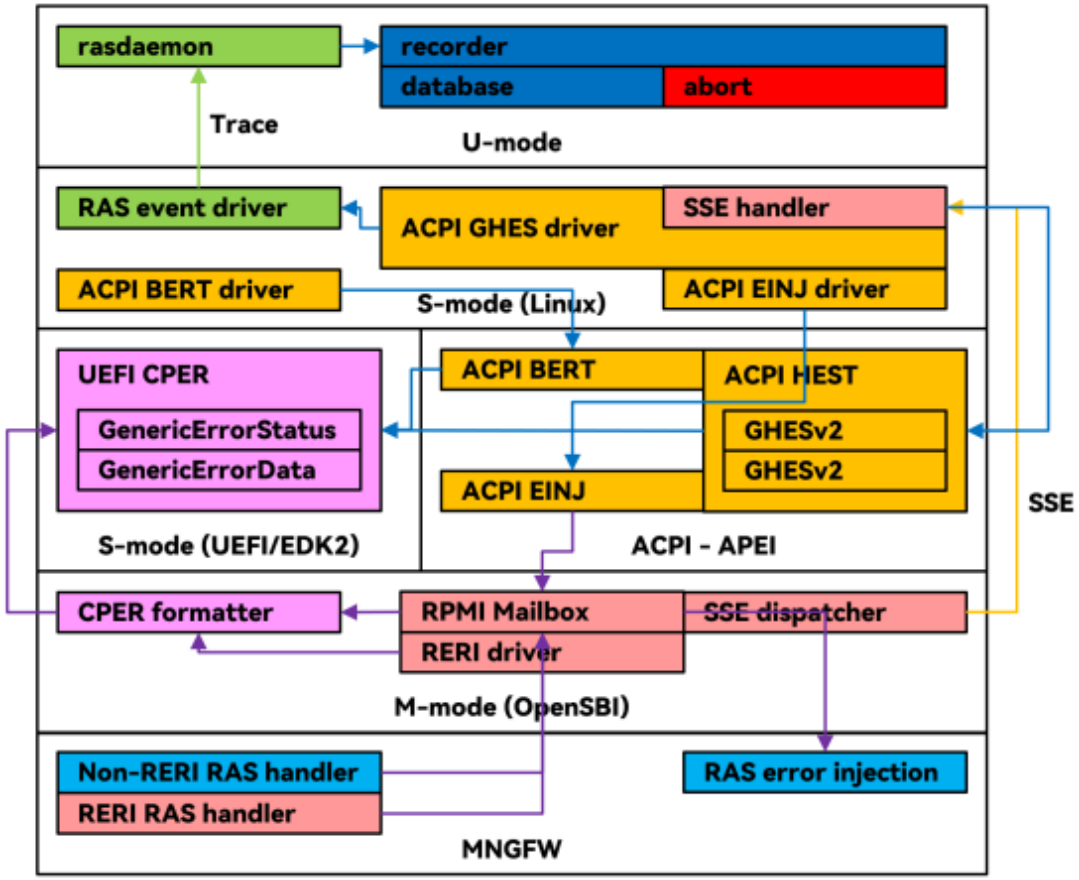
RISC-V Feature – RPMI

- RISC-V RPMI compliant mailbox
  - Support secure/non-secure world specific mailbox slots
  - Support 16KB per-world external SRAM based message channels
  - Support per-world P2A/A2P REQ/ACK doorbell interrupts
- Additional FIFO based mailbox
  - Support secure/non-secure world specific mailbox slots
  - Support up to 16 mailbox slots and up to 8 users per-world
  - Support 8*32-bit FIFO based message per-channel (slot)



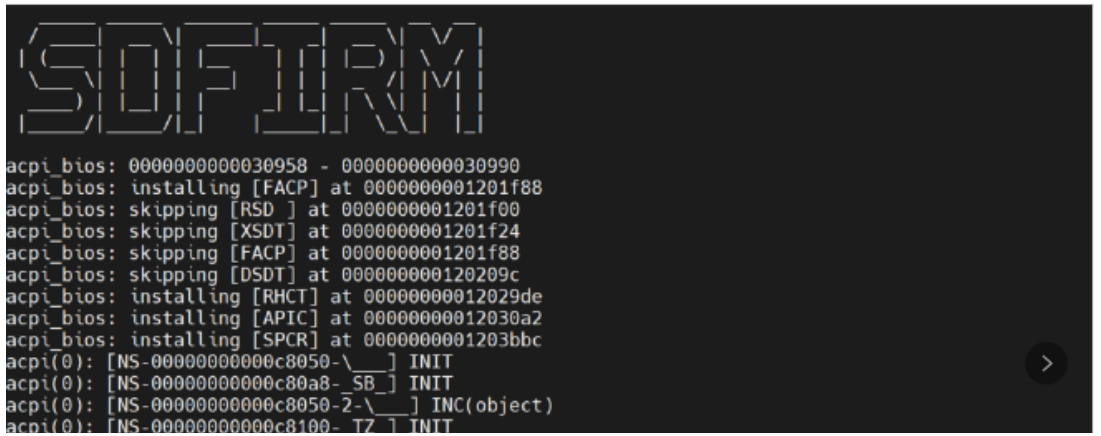
RAS Overview

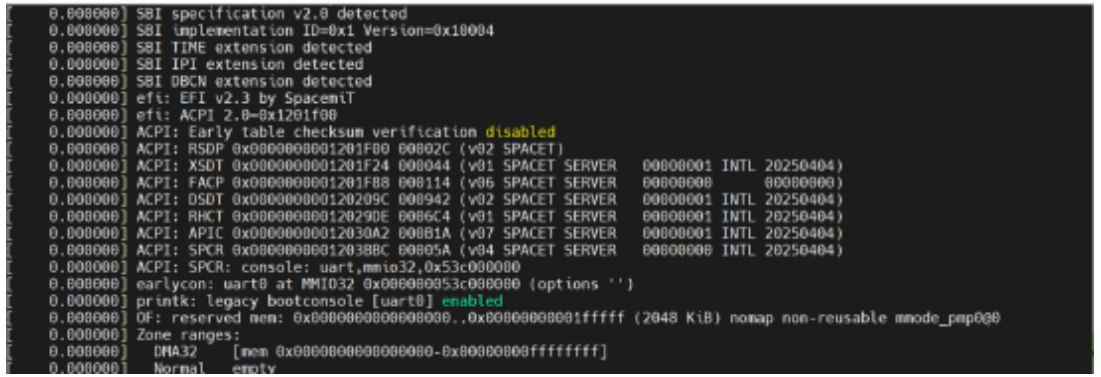
- RAS ACPI/APEI compliance
  - BERT
  - HEST
  - EINJ
- RAS EFI compliance
  - CPER
- RAS RISC-V compliance
  - RERI
  - RPMI
  - SSE
- Hardware RAS sources
  - CPU
  - IOMMU
  - DDR
  - PCIe
  - ECC SRAM



RAS Feature – ACPI/APEI

- Support pre-silicon stubbed EFI memory descriptor, system table and memory mapping embedded in SBI firmware
- Support pre-silicon lightweight ACPI tables embedded in SBI firmware
- Support compile time ACPI table modification via preprocessor
- Support runtime ACPI table modification via EFI SDTs (system definition tables) protocol in SBI firmware
  - Support SBI bootstrap fixup of ACPI data tables and SDTs
  - Support partial goods fixup of ACPI processor and interrupts in xSDTs
- Support automatic APEI/HEST table generation directly from RERI and other errors indirectly reported via RPMI





RAS Feature – CPU RERI

RERI Errors	CPER Error Type	CPER Error Severity	CPER Other Info
L2Cache SnoopFilter ECC Error (CE/UUE)	0x00: Unknown	2 – Corrected 1 - Fatal	Processor Type: RISC-V Processor ISA: RISC-V 64
L2Cache TAG ECC Error (CE/UUE)	0x01: Cache Error	2 – Corrected 1 - Fatal	
L2Cache DATA ECC Error (CE/UDE)	0x01: Cache Error	2 – Corrected 0 - Recoverable	
CoreX IFU Consume Poison (UUE)	0x00: Unknown	1 - Fatal	
CoreX ICACHE TAG Parity Error (CE)	0x01: Cache Error	2 - Corrected	
CoreX ICACHE DATA Parity Error (CE)	0x01: Cache Error	2 - Corrected	
CoreX jTLB TAG Parity Error (CE)	0x02: TLB Error	2 - Corrected	
CoreX jTLB DATA Parity Error (CE)	0x02: TLB Error	2 - Corrected	
CoreX LSU Consume Poison (UUE)	0x00: Unknown	2 – Corrected 1 - Fatal	
CoreX DCACHE TAG ECC Error (CE/UUE)	0x01: Cache Error	2 – Corrected 1 - Fatal	
CoreX DCACHE DATA ECC Error (CE/UCE)	0x01: Cache Error	2 – Corrected 0 - Recoverable	

RAS Feature – IOMMU RERI

Errors	CPER Error Type	CPER Error Severity	CPER Other Info
IOATS Configuration cache (CFGC) data parity and CRC	0x02: TLB Error	2 - Corrected	Control register Status register
IOATS Configuration cache (CFGC) tag parity and CRC	0x02: TLB Error	2 - Corrected	
IOATS 1st stage level-X page table walk cache (PTWC SLX) data parity and CRC	0x02: TLB Error	2 - Corrected	
IOATS 1st stage level-X page table walk cache (PTWC SLX) tag parity and CRC	0x02: TLB Error	2 - Corrected	
IOATS 2nd stage level-X page table walk cache (PTWC GLX) data parity and CRC	0x02: TLB Error	2 - Corrected	
IOATS 2nd stage level-X page table walk cache (PTWC GLX) tag parity and CRC	0x02: TLB Error	2 - Corrected	
IOATC Main TLB (MTLB) data parity and CRC	0x02: TLB Error	2 - Corrected	
IOATC Main TLB (MTLB) tag parity and CRC	0x02: TLB Error	2 - Corrected	

RAS Feature – DDR

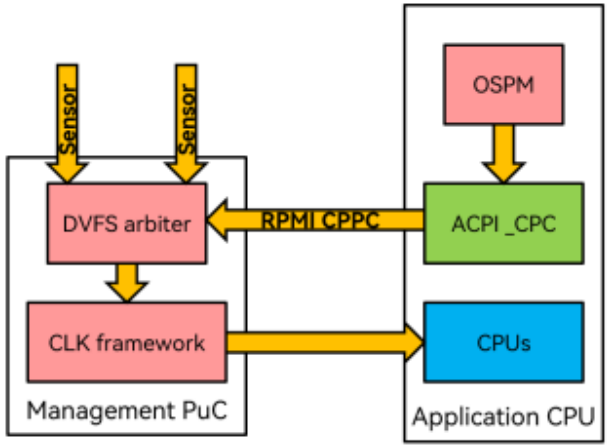
DDR Errors	CPER Error Type	CPER Error Severity	CPER Other Info
Derate temperature limit error	0 - Unknown	3 – Informational	Physical address Physical address mask Bank Row Column Rank Bit position Chip identification
Command error	0 - Unknown	0 - Recoverable	
Control update error	0 - Unknown	1 – Fatal	
Refresh management alert	0 - Unknown	3 – Informational	
ECC CE	2 - Single-bit ECC	2 – Corrected	
ECC UE	3 - Multi-bit ECC	1 – Fatal	
DDR write CRC error	8 - Parity Error	0 – Recoverable	
DDR write CRC err max reached error	8 - Parity Error	1 – Fatal	
DDR write CRC retry limit error	8 - Parity Error	1 – Fatal	
DDR read CRC max reached error	8 - Parity Error	1 – Fatal	
DDR read retry limit error	8 - Parity Error	1 – Fatal	
CA parity retry limit reached error	8 - Parity Error	1 – Fatal	
CA parity FATL error	8 - Parity Error	1 – Fatal	
Write Buffer CHI Port X RAM Y parity error	8 - Parity Error	0 – Recoverable 1 – Fatal	
Read Buffer CHI Port X RAM Y parity error	8 - Parity Error	0 – Recoverable 1 – Fatal	

RAS Feature – Others

Module	Error	CPER Error Type	CPER Error Severity	CPER Other Info
PCIe	PCIe advanced error reporting CE	PCIe AER Capability: • Physical Layer • Data Link Layer • Transaction Layer	2 – Corrected	Port Type Device ID Command Status Device Serial Number Capability Structure
	PCIe advanced error reporting UE		1 – Fatal	
SRAM	SEC event	2 - Single-bit ECC	2 – Corrected	Physical address Physical address mask Bit position
	DED event	3 - Multi-bit ECC	1 – Fatal	
BUS	SnoopFilter tag ECC (SECDED)	Corrected Error (CE) Deferred Error (DE)	2 – Corrected 0 – Recoverable	Error status Error addresses
	LLC tag ECC (SECDED)	Corrected Error (CE) Uncorrected Error (UE)	2 – Corrected 1 - Fatal	
	LLC data ECC (SECDED)	Corrected Error (CE) Deferred Error (DE)	2 – Corrected 0 – Recoverable	
	Error request type detect	Deferred Error (DE)	0 – Recoverable	
	AXI/ACE lite write data poison detect	Uncorrected Error (UE)	1 – Fatal	
	AXI/ACE lite write data error	Deferred Error (DE)	0 – Recoverable	
	AXI/ACE lite write response error (BRESP)	Uncorrected Error (UE)	1 – Fatal	

DVFS Feature – ACPI cpufreq

```
[   70.596095] riscv-aplic RSCV0002:00: 511 interrupts forwarded to MSI base 0x00
00000558600000
[   70.632310] ACPI CPPC: Parsed CPC struct for CPU: 0
[   70.666634] suspend: HSM suspend not available
[   70.692352] ACPI CPPC: Parsed CPC struct for CPU: 1
[   70.712284] suspend: HSM suspend not available
[   70.765939] ACPI CPPC: Parsed CPC struct for CPU: 4
[   70.786472] suspend: HSM suspend not available
[   70.814879] ACPI CPPC: Parsed CPC struct for CPU: 5
[   70.835528] suspend: HSM suspend not available
[   70.857715] ACPI CPPC:  Checking ACPI CPC validity
[   70.865554] ACPI CPPC:  CPU2 CPC descriptor is NULL
[   70.873616] ERST DBG: ERST support is disabled.
[   70.880993] SBI CPPC extension detected
[   70.886813] SBI MPXY extension not available
[   73.854227] Serial: 8250/16550 driver, 1 ports, IRQ sharing disabled
[   73.907865] printk: legacy console [ttyS0] disabled
[   73.926049] HISI0031:00: ttyS0 at MMIO 0x53c000000 (irq = 11, base_baud = 6250
00) is a 16550A
[   73.939818] printk: legacy console [ttyS0] enabled
[   73.939818] printk: legacy console [ttyS0] enabled
[   73.952866] printk: legacy bootconsole [uart0] disabled
[   73.952866] printk: legacy bootconsole [uart0] disabled
[   74.016096] suspend: HSM suspend not available
[   74.455415] CPPC Cpufreq: Initializing CPPC CPUfreq driver
[   74.463094] CPPC Cpufreq: Registering CPUfreq driver
[   74.472168] CPPC Cpufreq: Initializing CPU0
[   74.478716] CPPC Cpufreq: CPU0 performance caps - lowest: 40, lowest_nonlinear
: 40, nominal: 104, highest: 104
[   74.490338] CPPC Cpufreq: CPU0 frequency range - min: 1000000 kHz, max: 200000
0 kHz
[   74.499437] CPPC Cpufreq: CPU0 using independent policy
[   74.505989] CPPC Cpufreq: CPU0 fast_switch: disabled, dvfs_from_any_cpu: enabl
ed
[   74.514817] CPPC Cpufreq: CPU0 setting initial performance to 104 (freq: 20000
00 kHz)
[   74.525120] CPPC Cpufreq: CPU0 initialization completed successfully
```



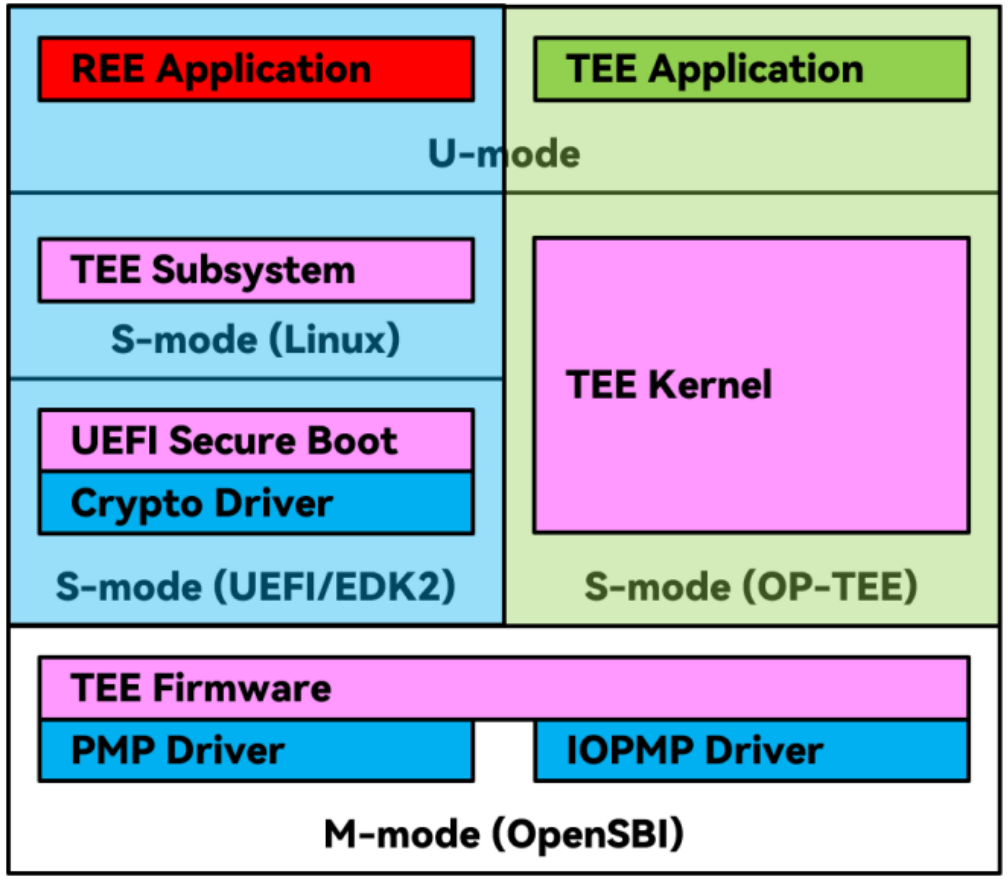
- Support ACPI CPPC (collaborative processor performance control)
- OSPM invokes _CPC control method in system definition tables
- RISC-V specific RPMI channel is used to send/receive CPPC request/response
- PuC firmware arbitrates frequency requests ceiling/floor, manipulates power and frequency using PID algorithm
- PuC firmware invokes clock tree management framework to manipulate CPU frequency dynamically

03

Security

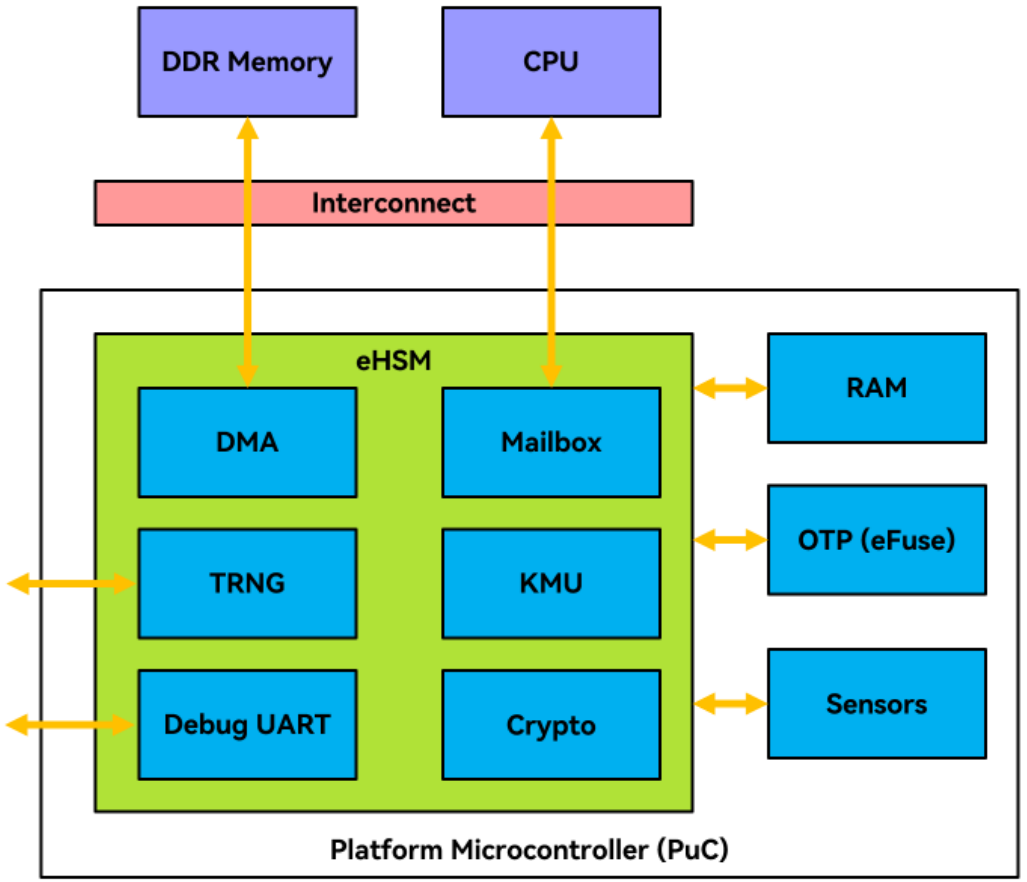
Security – PMP/IOPMP

- Support CPU secure enclave via up to 16 entries of PMP
- Support I/O secure enclave via IOPMP instantiated for each I/O subsystem, each instantiated IOPMP
  - Support up to 32 entries
  - Support up to 64 MD and totally up to 1024 entries
  - Support up to 1024 device IDs
- Support GP-TEE compliant TEE OS (OP-TEE)
- Support secure boot in UEFI and OpenSBI



Security – eHSM

- OSCCA (Office of the State Commercial Cryptographic Administration) Chinese commercial cryptography scheme - level 1 compliance
- Support running up to 600MHz frequency
- Support security algorithm of hashing, symmetric and asymmetric encryption
- Support key management utility (KMU) to store keys in OTP/RAM
- Support TRNG
- Support security sensors
  - Active shield
  - Temperature sensor
- Support secure debugging



04

Performance

Performance Monitors – CPU HPM

X100 Event			
Stalled-backend	Stalled-frontend	Branch-instructions	L1Dcache-loads
L1Dcache-stores	L1Dache-prefetches	Icache-accesses	Icache-prefetches
L2-loads	L2-stores	L2-prefetches	DTLB-loads
DTLB-stores	DTLB-prefetches	ITLB-accesses	Branch-misses
L1Dcache-load-misses	L1Dcache-store-misses	L1Dcache-prefetch-misses	L2-load-misses
L2-store-misses	L2-prefetch-misses	DTLB-load-misses	DTLB-store-misses
DTLB-prefetch-misses	ITLB-load-misses		

Performance Monitors – IOMMU HPM

IOATS Events	
Untranslated requests	Page table walk cache requests
Translated requests	Configuration cache misses
DTI_ATS translation requests	Page table walk cache misses
DTI_TBU translation requests	All translation requests
Device directory walks	All translations buffered
Process directory walks	Configuration cache lookups
1st stage page table walks	1st stage level-X page table walk cache lookups
2nd stage page table walks	1st stage level-X page table walk cache misses
DTI_ATS page requests (PRI)	2nd stage level-X page table walk cache lookups
Configuration cache requests	2nd stage level-X page table walk cache misses

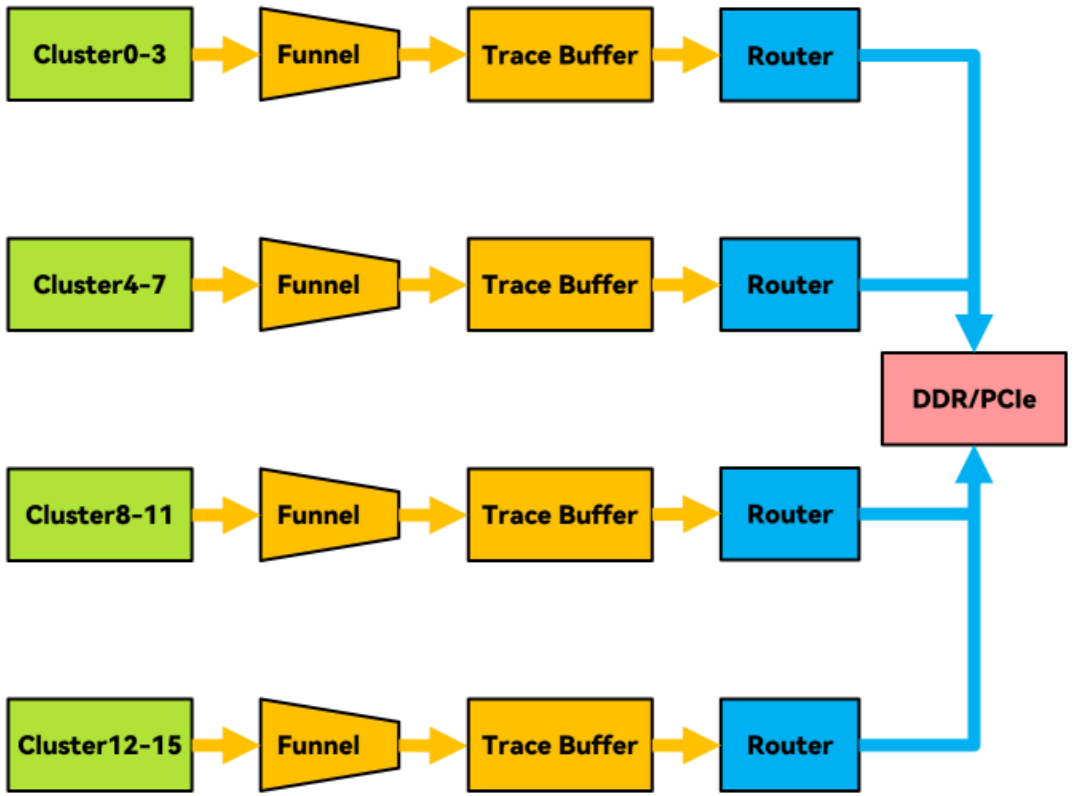
IOATC Events	
Untranslated (ATST=0) requests	Write transactions unissued of write buffer full
Translated (ATST=1) requests	Write transactions using write buffer
TLB misses	Write transactions not using write buffer
All translation requests	Main TLB (MTLB) lookups
Transactions issued	Main TLB (MTLB) misses
Transactions unissued of slot drain	Micro TLB (uTLB) lookups
Transactions unissued of token drain	

Performance Monitors - DDR

DPM Events	
Effective reads	Write combines
Effective writes	Visible window limitation reached reads
Bypass reads	Visible window limitation reached writes
Bypass activations	Scheduler allocations
DFI read data cycles	Scheduler starvations
DFI write data cycles	Channel based command counting
Type specific op counting	CHI requests dropped
Prioritized transactions when critical	WAR hazards
Precharges	RAW hazards
Read transitions	WAW hazards
Write transitions	

Tracers – CPU N-Trace

- Support RISC-V Nexus based trace (N-Trace) encoder and control interfaces
- Support APB and JTAG DP accesses of N-Trace control interfaces
- Support up to 312.5MHz CPU trace source frequency
- Support up to 300MHz trace channel frequency
- Support 32 depth FIFO based trace buffer
- Support routing trace data to memory and PCIe trace peripherals
- Support trace timestamping

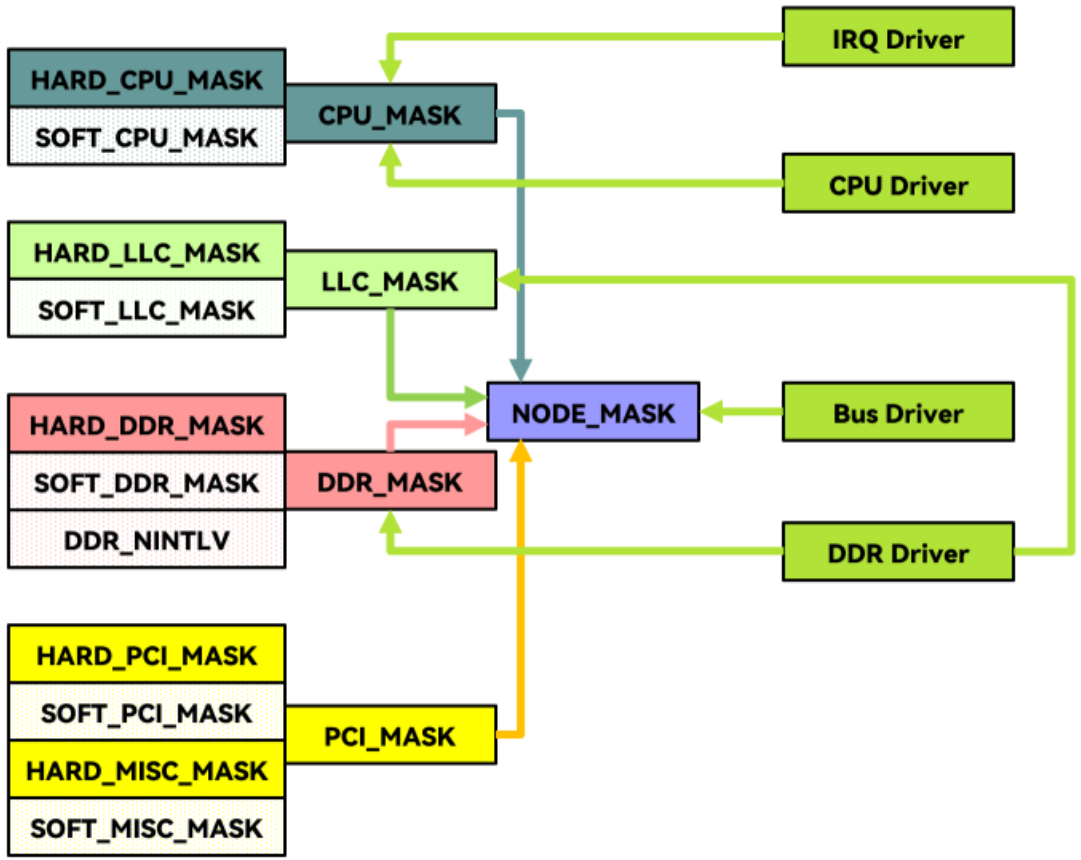


05

Other Features

Yield – Partial Goods

- Support ATE software calibration of CPU/LLC/DDR masks
- Support ATE hardware eFuse of CPU/LLC/DDR masks
- Support hardware integration of Big-Little CPU cores
- Support automatic hardware bus nodes enumeration
- Support pre-silicon various hardware simulation configurations

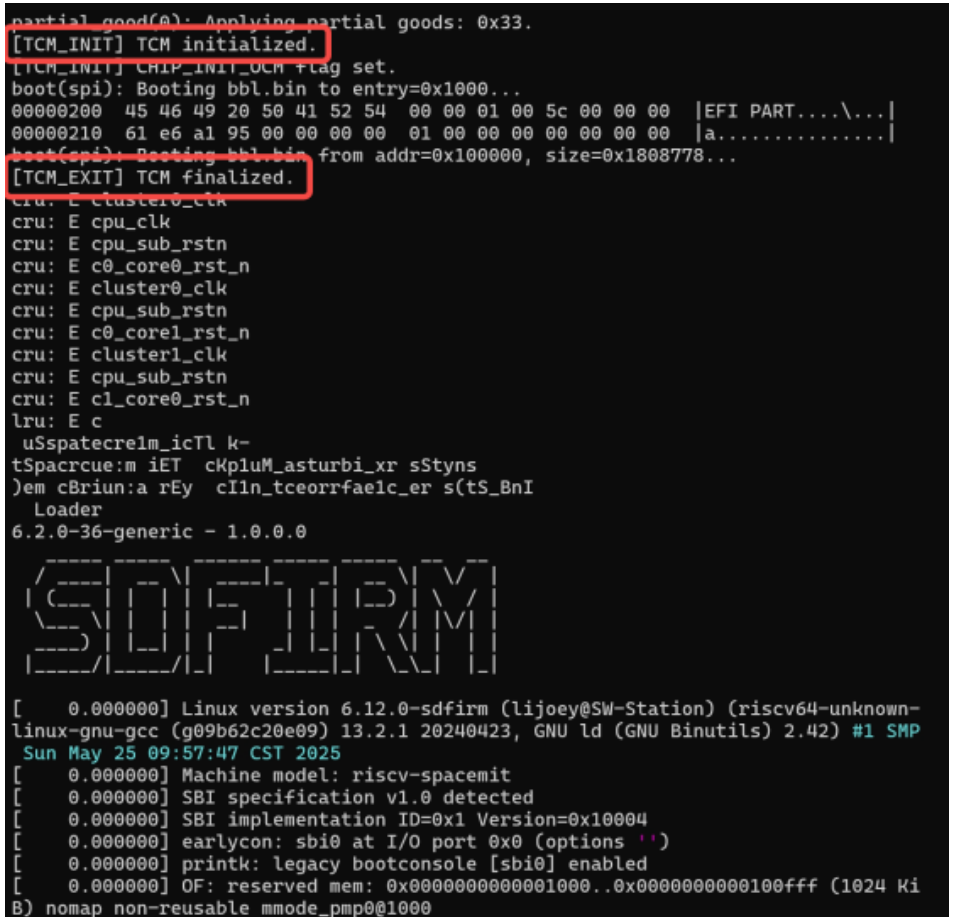


Yield – Partial Goods

- Support automatic software adaption of DDR interleave and cache groups configurations
- Support automatic software adaption of CPU clock and power gating
- Support automatic software fixup of device tree CPUs and interrupts
- Support automatic software fixup of ACPI firmware CPUs and interrupts
- Support Big-Little architecture to integrate community opensource cores

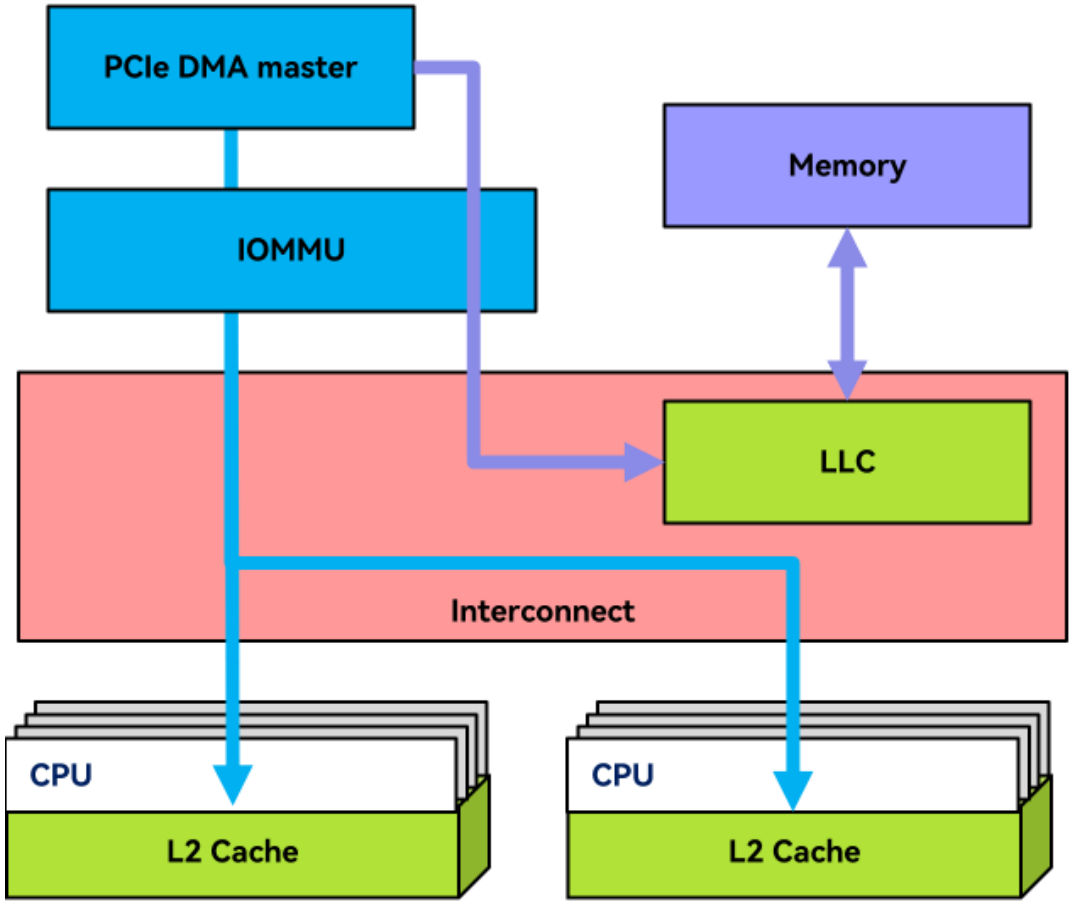
Bootstrap – TCM

- Boot EFI BIOS to DDR address space while still can have DDR driver in the BIOS
  - Configure TCM as memory located in the very first segment of DDR memory regions
  - Reconfigure TCM as CPU cache and leave memory regions for DDR
  - DDR driver runs between TCM initialization and finalization
- Run post-silicon tests by using TCM while DDR is not available
  - Run rich-featured ATE functional test patterns using TCM while can still save silicon area with limited SRAM
  - Reduce TTM during post-silicon validation by running operating system tests using TCM prior to DDR availability



Data Plane – Cache Stashing

- Support CHI snoop style dataless cache stashing transactions directed to L2 cache in X100 CPU cluster
  - SnpUniqueStash
  - SnpMakeInvalidStash
  - SnpStashShared
  - SnpStashUnique
- Support pass-through CHI dataless cache stashing transactions in T100 IOMMU
  - WriteUniquePtlStash
  - WriteUniqueFullStash
  - StashOnceShared
  - StashOnceUnique
- Support CHI dataless cache stashing transactions in PCIe controllers
  - WriteUniquePtlStash (TH=1)



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Thanks

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